

Abstract

Low power architecture features and techniques are provided in a scalable array indirect VLIW processor. These features and techniques include power control of a reconfigurable register file, conditional power control of multi-cycle operations and indirect VLIW utilization, and power control of VLIW-based vector processing using the ManArray register file indexing mechanism. These techniques are applicable to all processing elements (PEs) and the array controller sequence processor (SP) to provide substantial power savings.